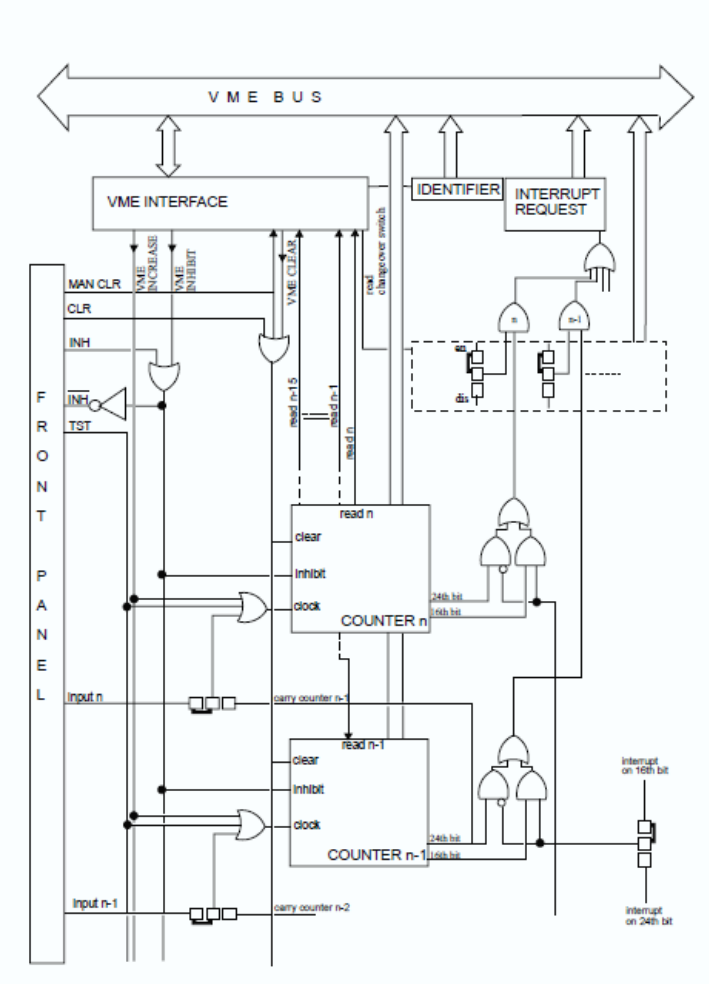
Rev.1 - 25/06/1999

V260

16 Channel Scaler



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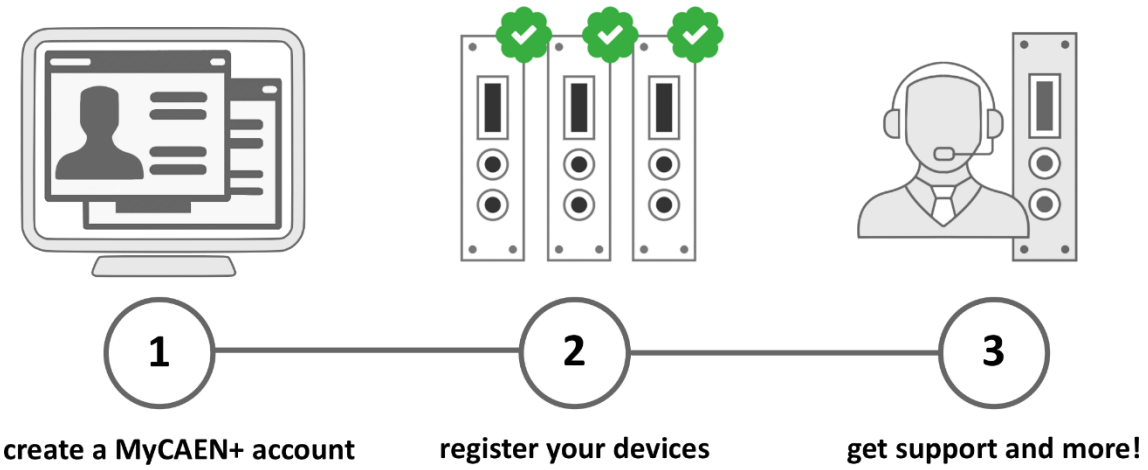

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Technical Information Manual

Version 1.0

25 June 1999

MOD. V 260

16 CHANNEL
SCALER

CAEN will repair or replace any product within the guarantee period if the Guarantor declares that the product is defective due to workmanship or materials and has not been caused by mishandling, negligence on behalf of the User, accident or any abnormal conditions or operations.

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Disposal of the Product

The product must never be dumped in the Municipal Waste. Please check your local regulations for disposal of electronics products.

Table of Contents

1. DESCRIPTION

1.1 FUNCTIONAL DESCRIPTION (refer to figure 1)

The model V 260 is a 1-unit wide VME module provided with 16 independent 24-bit counting channels operating at the guaranteed input frequency of 100 MHz. The module houses a VME RORA INTERRUPTER[1] that generates a VME interrupt (if enabled) whenever the "interrupt bit" of a channel becomes true.The "interrupt bit" may be the 24th or the 16th; two jumpers are dedicated to selection of the "interrupt bit" for channels 0..7 and channels 8..15.

Each channel is provided with two internal jumpers by which it is possible:

to connect the channel itself to the preceding one: each channel adds a 24-bit counting capacity to the previous one. In this way various scale configurations are available; in particular it is possible to implement a single (24 x 16)-bit multichannel scale.

to enable/disable the interrupt generation.

Operation of the module is fully controlled via VME. Some operations can be also performed by three external NIM signals (indicated on the front panel connector with "INH","CLR", "TST"):

INH: (INHIBIT) an input signal sent through this connector disables the counting.

CLR: (FAST CLEAR) an input signal present on this connector resets all the channels (it is possible to perform the same operation by pressing the "MAN CLR" push-button located on the front panel).

TST: (TEST) if the module is configured with 16 independent channels, a signal sent through this connector increases all the channels.

The front panel LED "$\overline{\text{INH}}$" is off when the module is in the INHIBIT state.

The module V 260 is an A24 D16/32 VME slave; its Base address is fixed by 4 internal rotary switches. A front panel LED (SEL) lights up each time the module generates the VME signal DTACK.

The module is available in three different versions:

V260 E, differential ECL inputs
V260 N, NIM inputs
V260 T, TTL inputs

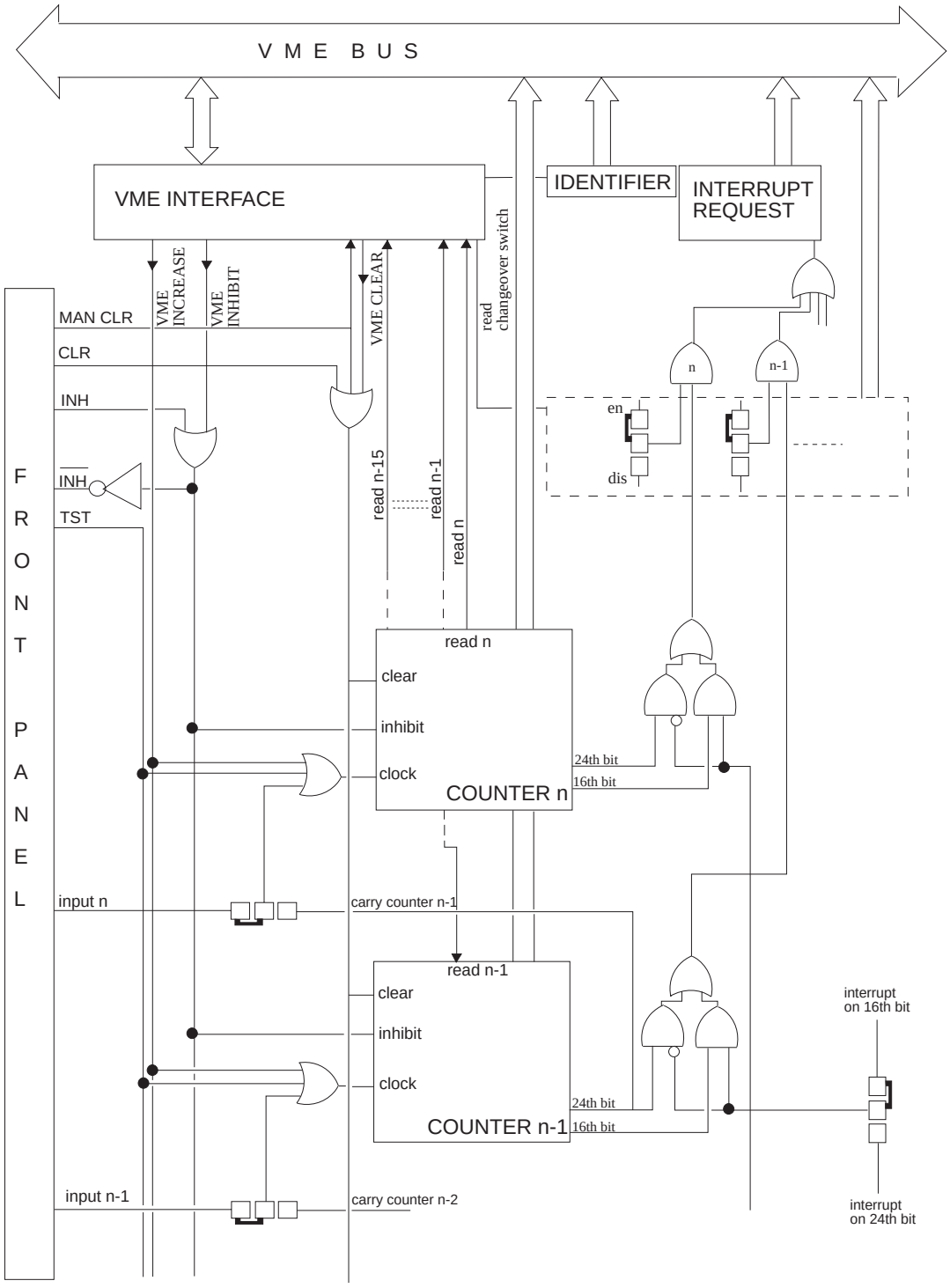


Figure 1 Functional Block Diagram of the Module V 260

2. SPECIFICATIONS

2.1 PACKAGING

1-unit wide VME unit.

2.2 EXTERNAL COMPONENTS

CONNECTORS

- No.2, "INPUTS 0..7", "INPUTS 8..15", 16 pin lead flat cable connector, 110Ω impedance; for the 16 input channels (ECL version).

- No.16, "INPUTS 0..15", LEMO 00 type, 50 Ω impedance; for the input signals (for NIM and TTL version).

- No.1, "TST", LEMO 00 type, 50 Ω impedance; for the TEST input signals (ECL, NIM and TTL version).

- No.1, "CLR", LEMO 00 type, 50 Ω impedance; for the FAST CLEAR input signals (ECL, NIM and TTL version).

- No.1, "INH", LEMO 00 type 50 Ω impedance. Connector for the INHIBIT input signals (ECL, NIM and TTL version).

LEDs

- No.1, "SEL", red, VME Selected; it lights up during a VME access.

- No.1, "$\overline{\text{INH}}$", green, not INHIBIT led; signalling, when alight, the absence of the INHIBIT signal. The scales are able to count.

SWITCHES

- No.1, "MAN CLR", manual clear push-button; by pushing this button:

- all the counting scales are cleared;

- the VME interrupt request (if asserted) is removed;

- the VME interrupt generation are disabled.

- the VME INHIBIT are cleared.

2.3 INTERNAL COMPONENTS

(refer to Appendix C - components location)

JUMPERS

- No.2, "JP17", "JP18". These jumpers are dedicated to the selection of the "interrupt bit" for channels 0..7(JP18) and channels 8..15 (JP17):

jumper inserted : interrupt on 24th bit

jumper removed : interrupt on 16th bit

SWITCHES

- No.16, changeover switches (group JP1..JP16). For cascading the relative channels to the preceding one.

- No.16, changeover switches (group JP1..JP16). For enabling/disabling the interrupt generation of the corresponding channel.

- No.4, rotary switches for the module VME Base address selection.

- No 3, dip-switches, "SW1..3" . These dip-switches allow the selection of the VME interrupt level.

FUSES

- No.1, fuse 5 A, +5 V.

- No.1, fuse 2 A, -12 V.

2.4 POWER REQUIREMENTS

+ 5 V	1.8 A
- 12 V	220 mA (for ECL and NIM versions)

2.5 CHARACTERISTICS OF THE SIGNALS

- INPUT CHANNELS:	std. NIM or TTL level , 50 Ω impedance;
	std. differential ECL level, 110 Ω impedance;
	max. frequency:110 MHz; min. width 5 ns;
	min. time interval between two pulses: 5 ns.
- INHIBIT:	std. NIM level, 50 Ω impedance;
	min. width 50 ns; it must precede the input channel signal by 35 ns.
- CLEAR:	std. NIM level, 50 Ω impedance; min. width: 60 ns.
- TEST:	std. NIM level, 50 Ω impedance; max. frequency: 50 MHz;
	min. width: 10 ns.

3. OPERATING MODES

3.1 COUNTING SCALES

The module V 260 houses 16 independent 24-bit channels that can be cascaded by internal changeover switches in order to obtain various scale configurations with equal or different counting capacities.

The figure on the following page shows the changeover switches' location and position for the different operating modes.The clock changeover switch allows the connection of a channel to the preceding ones, or to the corresponding input:

If channel n is not connected to the preceding one, its clock is the external input n.

If channel n is connected to the preceding one, its clock is the 24th bit of channel n-1; (channel 0 can be connected to channel 15).

For example, a 72-bit scale is obtained by connecting channel 3 with channel 4 and channel 4 with channel 5: in this case the module is configured with:

- one 72-bit scale (channel 3,4,5); it receives the input signal through the input 3 connector and its MSB is the 24th bit of channel 5;
- thirteen 24-bit scale (channel 0,1,2,6..15).

3.2 INTERRUPT GENERATION

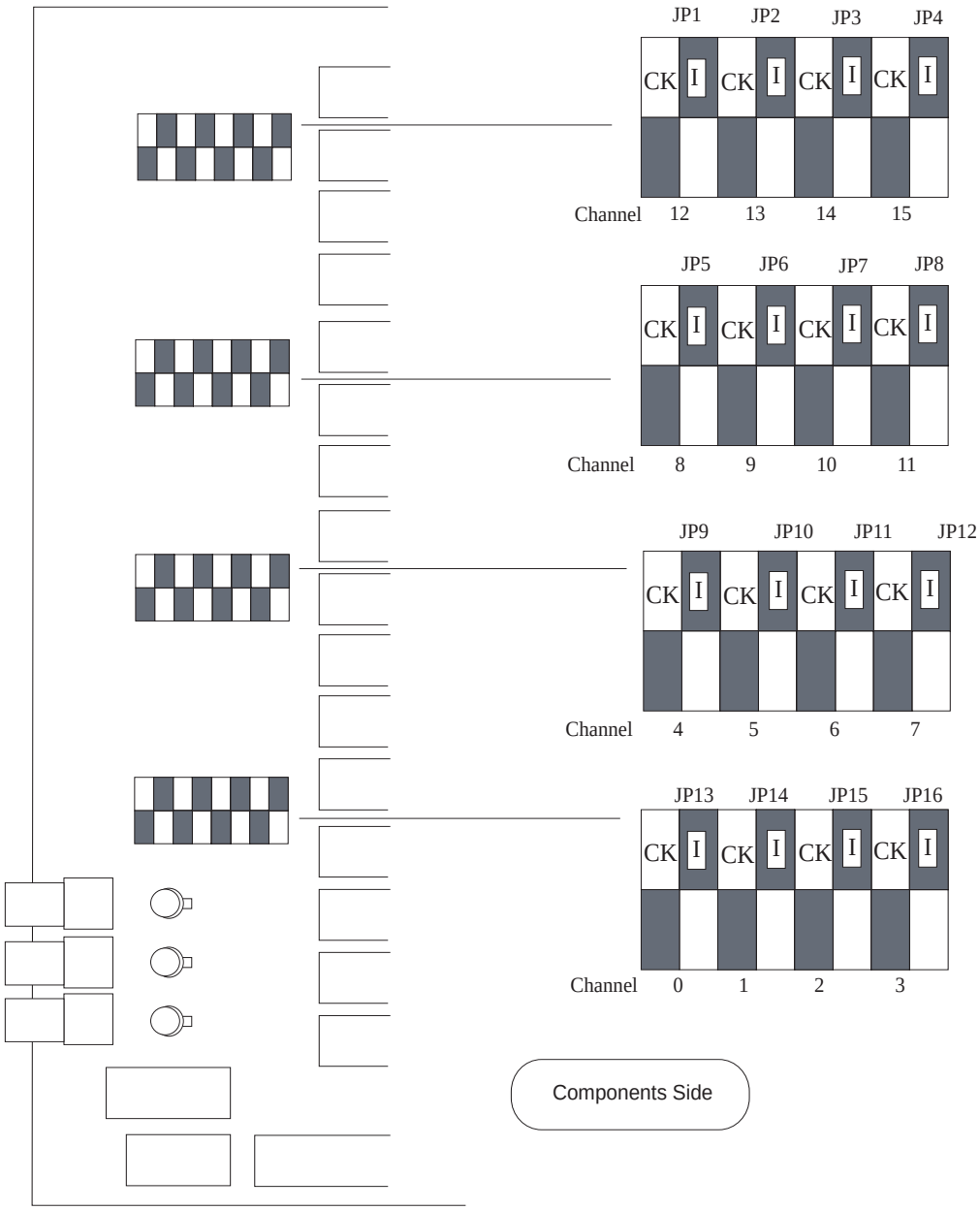
For each channel a corresponding changeover switch, see figure on following page, enables/disables the interrupt generation.

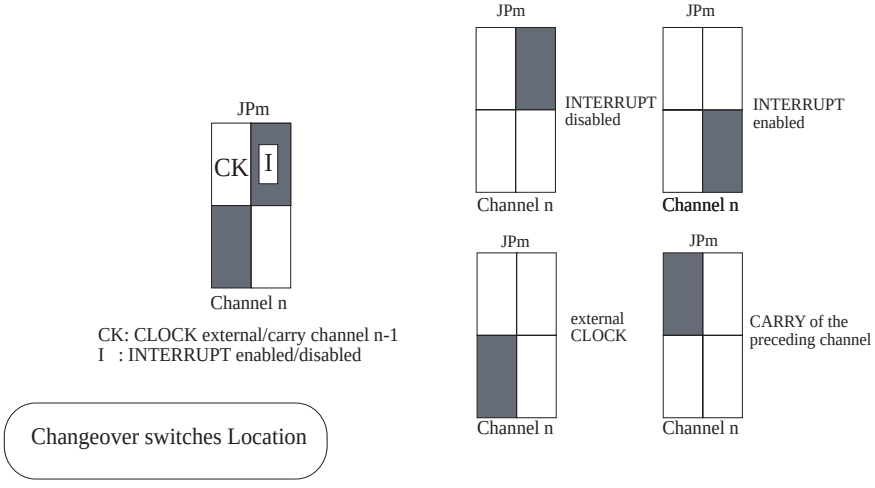
It is possible to read the state of these changeover switches via VME (see paragraph 4.4).

The Mod. V260 (if enabled; see paragraph 5) generates a VME interrupt whenever the "interrupt bit" of an enabled channel becomes true.

Two jumpers, JP17 and JP18 (see Appendix C - Components Location) allow the "interrupt bit " settings:

If JP18 is present	channel 0..7 "interrupt bit"	= 24th bit.
If JP18 is removed	channel 0..7 "interrupt bit"	= 16th bit.
If JP17 is present	channel 8..15 "interrupt bit"	= 24th bit.
If JP17 is removed	channel 8..15"interrupt bit"	= 16th bit.


JP1
JP2
JP3
JP4
CK
I
Channel 12 13 14 15
JP5
JP6
JP7
JP8
Channel 8 9 10 11
JP9
JP10
JP11
JP12
Channel 4 5 6 7
JP13
JP14
JP15
JP16
Channel 0 1 2 3
Components Side


JPm
CK
I
Channel n
CK: CLOCK external/carry channel n-1
I : INTERRUPT enabled/disabled
INTERRUPT disabled
INTERRUPT enabled
external CLOCK
CARRY of the preceding channel
Changeover switches Location

There is no difference in the interrupt generation if an enabled channel belongs to a multi-channel scale: whenever its "interrupt bit" is asserted, the interrupt is generated;

(If the interrupt generation is desired on the last bit of a multichannel scale; only the last channel has to be enabled)).

3.3 SCALE INHIBIT

It is possible to inhibit the scales count in this way:

- by sending a NIM signal through the "INH" connector located on the front panel.

- by setting the VME INHIBIT (access to the address Base +%52; see par. 4).

3.4 SCALE CLEAR

All the scales are cleared in the following cases:

- by sending a NIM signal through the "CLR" connector located on the front panel;

- by pushing the front panel push-button "MAN CLR";

- by accessing via VME the address Base + %50 (VME CLEAR).

3.5 CHANNEL TEST

If the module is configured with 16 independent channels it is possible to increment all channels:

- by sending a NIM signal through the "TST" connector located on the front panel.

- by accessing via VME the address Base + % 56.

3.6 MODULE CONFIGURATION

The module is supplied by CAEN with the internal jumpers as shown in Appendix C and Figure on page 6.

In this configuration each channel is an independent 24-digit counting scale and does not generate VME Interrupt.

At power-on:

all the scales are cleared;

VME INHIBIT is cleared; if there is no external INHIBIT the LED "INH" is on;

VME interrupt disabled.

4. VME INTERFACE

4.1 ADDRESSING CAPABILITY

The module works in A24 mode. This means that the module address must be specified in a field of 24 bits. The Address Modifiers used by the module are

AM =%39: standard user data access
AM =%3A: standard user program access
AM =%3D: standard supervisor data access
AM =%3E: standard supervisor program access

The module's Base Address is fixed by 4 internal rotary switches housed on a piggy-back board plugged into the main printed circuit board (the rotary switch with the least significant figure is situated near pin 1 of the piggy back board as shown in Appendix C; see also appendix A).

The Base Address can be selected in the range: % 00 0000 <-> FF FF00

The Base Address reserves in this way a page of 256 bytes for the module. The address map of the page is shown in table 4.1 on the following page.

Table 4.1 Address Map for the Mod. V 260		
ADDRESS	**REGISTER/CONTENT**	**TYPE**
Base + %FE Base + %FC Base + %FA	Version & Series Manufacturer & module type Fixed code	read only read only read only
Base + %F8.....Base + %5A	Not used	
Base + %58 Base + %56 Base + %54 Base + %52 Base + %50 Base + %4C Base + %48 Base + %44 Base + %40 Base + %3C Base + %38 Base + %34 Base + %30 Base + %2C Base + %28 Base + %24 Base + %20 Base + %1C Base + %18 Base + %14 Base + %10	Interrupt jumper status Scale increase INHIBIT reset INHIBIT set CLEAR scales Counter 15 Counter 14 Counter 13 Counter 12 Counter 11 Counter 10 Counter 9 Counter 8 Counter 7 Counter 6 Counter 5 Counter 4 Counter 3 Counter 2 Counter 1 Counter 0	read only read/write read/write read/write read/write read only read only read only read only read only read only read only read only read only read only read only read only read only read only read only read only
Base + %0E Base + %0C Base + %0A Base + %08 Base + %06 Base + %04	Not used CLEAR VME interrupt DISABLE VME interrupt ENABLE VME interrupt Interrupt level Interrupt vector	read/write read/write read/write read only write only
Base + %02 Base + %00	Unused Unused	

4.2 DATA TRANSFER CAPABILITY

The module has the following data transfer capability:

the internal registers are accessible in D 16 mode;

the counters are accessible in D 16/ D32 mode.

This means that the counters can be read either by Word or Long Word instructions while the register can be read by Word instructions only.

4.3 MODULE IDENTIFIER WORDS

The Three words located at the highest address on the page are used to identify the module as shown in figure 4.2:

Figure 4.2 Module Identifier Words

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	ADDRESS
VERSION				MODULE'S SERIAL NUMBER												Base + %FE
MANUFACTURER NUMBER								MODULE TYPE								Base + %FC
%FA FIXED CODE								%F5 FIXED CODE								Base + %FA

At the address Base + % FA the two particular bytes allow the automatic localisation of the module.

For the Mod.V260 the word at address Base + % FC has the following configuration:

Manufacturer N° = 000010 b

Type of module = 0000001101 b NIM version

= 0000001110 b TTL version

= 0000001111 b ECL version

The word located at the address Base + FE identifies the single module via the module's serial number and any change in the hardware, (for example the use of faster logic) will be shown by the Version number. These registers are accessible on WORD boundary only.

4.4 INTERRUPT CHANGEOVER SWITCHES STATUS

This read only register contains the status of the 16 changeover switches for the

enable/disable interrupt of the 16 channels.

If bit n = 1 the VME interrupt (if enabled) is generated when the "interrupt bit " of the corresponding channel n becomes true.

If bit n = 0 the channel n is not able to cause the VME interrupt.

Figure 4.3 Interrupt Jumper Status

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	ADDRESS
en 15	en 14	en 13	en 12	en 11	en 10	en 9	en 8	en 7	en 6	en 5	en 4	en 3	en 2	en 1	en 0	Base + %58

4.5 INHIBIT SET/RESET

A VME access (read or write) to the address Base + % 52 sets the VME INHIBIT; the scales are not able to count and the front panel LED "$\overline{\text{INH}}$" turns off.

A VME access (read or write) to the address Base + % 54 clears the VME INHIBIT; If no external INHIBIT is present, the scales are able to count and the front panel LED "$\overline{\text{INH}}$" turns on.

4.6 SCALE INCREMENT

If the module is configured with 16 independent channels, a VME access (read or write) to the address Base + 56 increases all the channels (same as the TST signal).

4.7 CLEAR SCALES

A VME access (read or write) to the address Base + % 50 causes the following operation:

- clears all the scales;
- removes the VME interrupt request (if asserted), (RORA INTERRUPTER);
- disables the VME interrupt generation.

4.8 COUNTERS

There are sixteen 32 bit read only registers. They contain the 24 bit value of the corresponding counting channel and one bit that shows the INHIBIT status. The structure of these registers is shown in figure 4.4 (bits 24 to 30 are not used and are read as "one" on the VME data

bus).

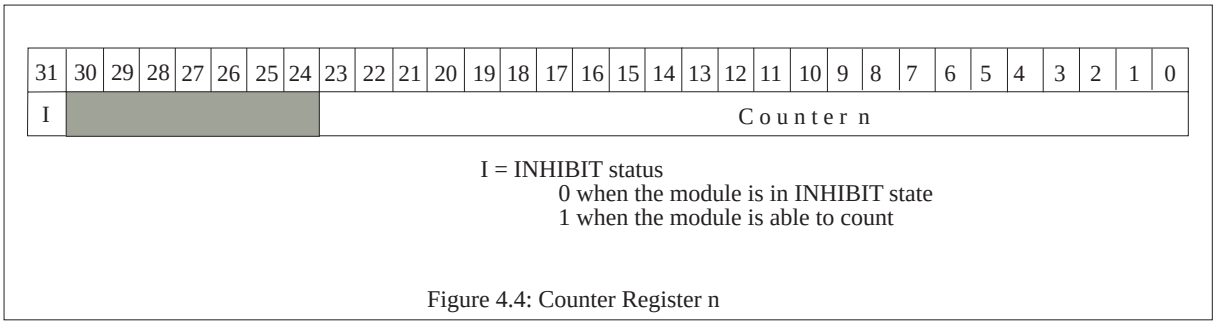


Figure 4.4: Counter Register n

These registers can be read in D16/D32 mode.When the D16 mode is used (word cycles) the register content is located on the 16 bit data bus following Motorola standard, i.e. the most significant word is located at the lowest VME addresses. The Figs 4.4 and 4.5 show how the counter value is located on the data bus in the two different cases.

During word cycle the counter value is latched during the access at the lowest addresses.

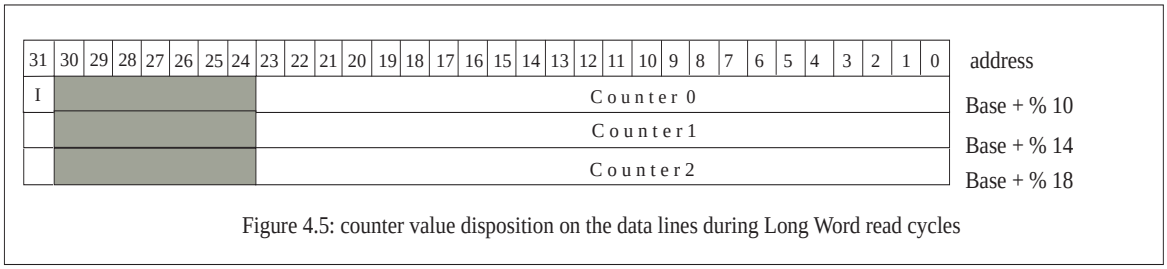


Figure 4.5: counter value disposition on the data lines during Long Word read cycles

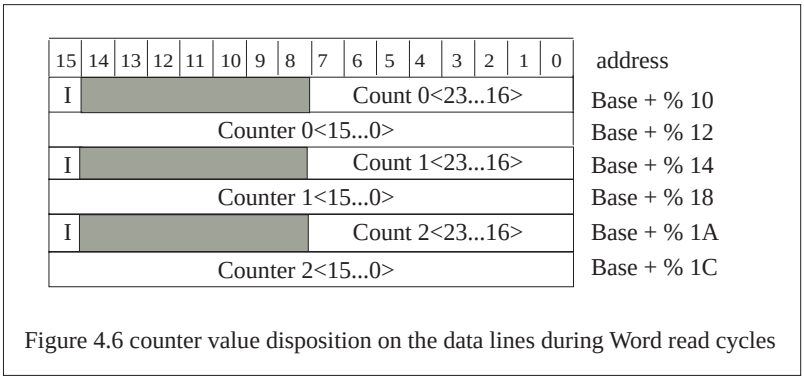


Figure 4.6 counter value disposition on the data lines during Word read cycles

4.9 CLEAR VME INTERRUPT

A VME access (read or write) to the address Base +% 0C removes the VME interrupt request (if asserted)(RORA INTERRUPTER).

4.10 ENABLE/DISABLE VME INTERRUPT

A VME access (read or write) to the address Base +% 08 enables the VME interrupt generation.

A VME access (read or write) to the address Base +% 0A disables the VME interrupt generation.

4.11 INTERRUPT LEVEL REGISTER

This read only register contains the value of the interrupt level set on the 3 internal dip switches.

The bit 0..2 correspond to SW1..3 as shown in the following figure:

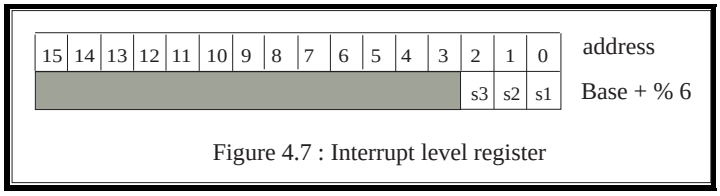


Figure 4.7 : Interrupt level register

4.12 INTERRUPT VECTOR REGISTER

The value written in this 8 bit write only register is the STATUS/ID that the V260 INTERRUPTER places on the VME data bus during the interrupt acknowledge cycle.

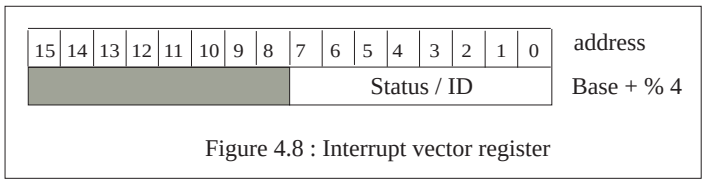


Figure 4.8 : Interrupt vector register

5.MOD. V260 INTERRUPTER

5.1 INTERRUPTER CAPABILITY

The Mod. V260 houses a VME RORA INTERRUPTER D08(o) type.This means that :

it responds to 8 bit, 16 bit and 32 bit interrupt acknowledge cycles providing an 8-bit STATUS/ID on the VME data lines D00..D07;

it removes its interrupt request when some on board registers are accessed by a VME MASTER (RORA: Release On Register Access).

5.2 INTERRUPT LEVEL

The interrupt level corresponds to the value set on the three dip-switches SW1..SW3 as described in the following figure. It is possible to read via VME the value at address Base + % 06.

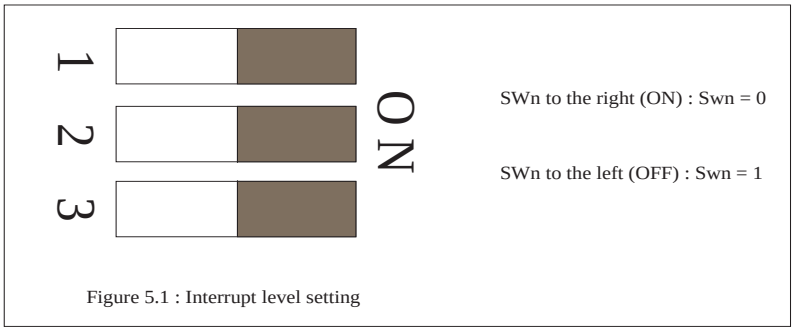


Figure 5.1 : Interrupt level setting

5.3 INTERRUPT STATUS/ID

The interrupt STATUS/ID is 8 bit wide, and it is possible to set its value via VME by writing at address Base + % 04.

5.4 INTERRUPT REQUEST RELEASE

The V260 INTERRUPTER removes its interrupt request in these cases:

by accessing the address Base + % 0C

by accessing the address Base + % 50

by pushing the front panel push-button "MAN CLR".

5.5 ENABLE/DISABLE INTERRUPT GENERATION

It is possible to enable/disable the Mod. V260 interrupt generation in the following way.

enable: by accessing the address Base + % 08.

disable: by accessing the address Base + % 0A;

by accessing the address Base + % 50;

by pushing the front panel push-button "MAN CLR".

5.6 INTERRUPT SEQUENCE

if the VME interrupt generation is enabled (access to the address Base + % 08):

{

- if the "interrupt bit" of an enabled channel becomes true and the value of the interrupt level set on SW1..SW3 is different from 0:

{

- It requests interrupt by driving an interrupt request line IRQ1..7 low according to the SW1..3 value;

- during the following acknowledge cycle it places on the VME data lines D00..D07 the STATUS/ID; it is the byte contained in the Interrupt vector register (address Base +% 04);

}

- if a VME MASTER accesses (read or write) the address Base +% 0C it releases its VME inter rupt request line;

- if a VME MASTER accesses (read or write) the address Base +% 50:

{

- it releases its VME interrupt request line;

- it clears all the scales;

- it disables the VME interrupt generation;

}

}

6. REFERENCES

VMEbus Specification Manual Revision C.1 October 1985

APPENDIX A

CHARACTERISTICS OF THE ADDRESS DECODING SUBSYSTEM

The MSB of the address (A23 to A4) are decoded in this subsystem. The 16 bits A23 to A8 are used to define the base address of the module and reserve in this way a page of 256 bytes for each module. The following 4 bits are decoded in a demultiplexer which generates 16 signals defining the internal groups of 16 bytes (GR0...GR15). The organization of the address decoding subsystem is shown in the figure.

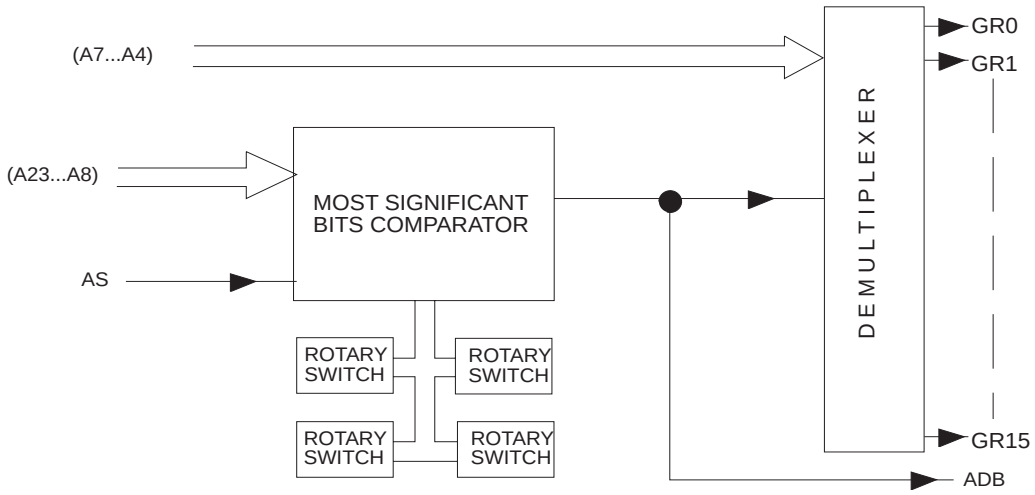


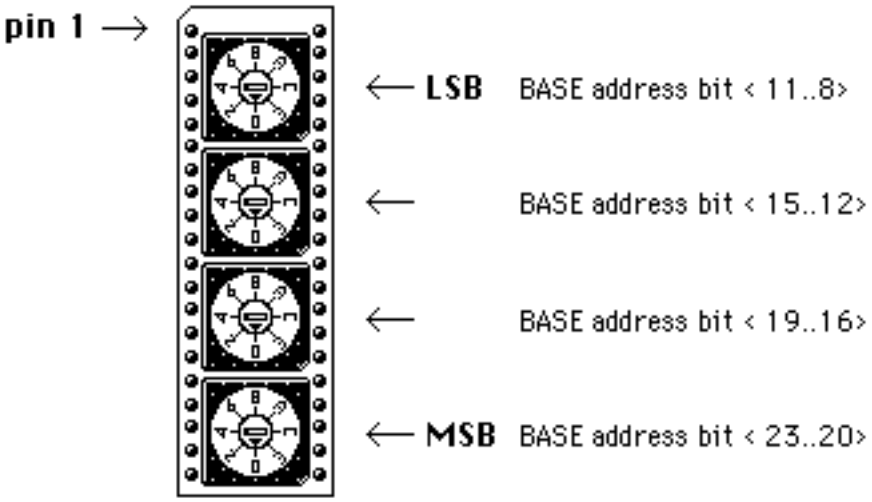
Figure A1 : Organization of the address decoding subsystem

The three remaining address bits (A3 to A1), and all the exchange signals with the VMEbus, will be treated in the circuits which are specific for each module).

Base decoding of the module's address

The decoding of the module's base address is performed by using two comparators 74F521 that comparate the value sets on the four hexadecimal rotary switches with the value of the VME address lines A23 to A8. The comparison is enabled by the AS signal to generate the base address signal (ADB). This signal indicates that the module is accessed by VME.

Each rotary switch sets the value of 4 bits of the module's base address. Figure A.2 on the following page shows the correspondence between the switches and the address bits.



Decoding of the internal groups

The address lines A7 to A4 are demultiplexed in 16 groups of 16 bytes each, by 2 74LS138 circuits enabled by the base address (ADB). They generate the 16 signals GR0...GR15.

Appendix B : Electrical Diagrams

Appendix C : Components List and Location

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