Device Modeling Report

COMPONENTS : BIPOLAR OPERATIONAL AMPLIFIER

PART NUMBER : NJM4558

MANUFACTURER : NEW JAPAN RADIO CO.,LTD

Version : 2

JRC 新日本無線株式會社

Spice Model
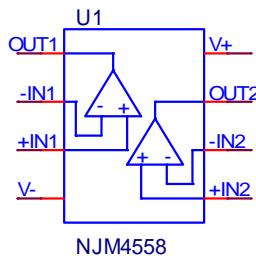

```
*$
*PART NUMBER:NJM4558
*BIPOLAR OPAMP
*Version:2
*Please note that the inaccuracy is involved to it when you use this model.
*Please refrain from the model's resale.
****************************************************************
*Model Generated by NEW JAPAN RADIO CO.,LTD *
*              All Rights Reserved                    *
*     Commercial Use or Resale Restricted             *
****************************************************************
.SUBCKT NJM4558 OUT1 -IN1 +IN1 V- +IN2 -IN2 OUT2 V+
X1 +IN1 -IN1 V+ V- OUT1 njm4558_s
X2 +IN2 -IN2 V+ V- OUT2 njm4558_s
.ENDS NJM4558
*$
* connections:     non-inverting input
*                   |  inverting input
*                   |  |   positive power supply
*                   |  |   |  negative power supply
*                   |  |   |  |   output
*                   |  |   |  |   |
*                   |  |   |  |   |
.subckt njm4558_s 1  2   3  4   5
C1 11 12 {C1}
C2 15 16 {C2}
CE 10 0 {CE}
RE 10 0 {RE}
D1 16 17 DMOD1
D2 17 16 DMOD1
D3 5 18 DMOD2
D4 19 5 DMOD2
D5 10 20 DMOD2
VTL 3 20 {VTL}
GB 16 0 15 0 {GB}
GA 15 0 11 12 {GA}
GC 0 17 5 0 {GC}
GCM 0 15 10 0 {GCM}
ITL 3 10 {ITL}
```

```
Q1 11 2 13 PNP1
Q2 12 1 14 PNP2
RO1 16 5 {RO1}
RC 17 0 {RC}
RO2 16 0 {RO2}
R2 15 0 100E3
RC1 11 21 {RC1}
RC2 12 22 {RC1}
VRC1 21 4 {VRC}
VRC2 22 4 {VRC}
RE2 10 14 {RE1}
RE1 10 13 {RE1}
ICE 3 4 {ICE}
RP 3 4 {RP}
VE 19 4 DC {VE}
VC 3 18 DC {VC}

.MODEL DMOD1 D(T_MEASURED = 25 IS = 5.41E-28)
.MODEL DMOD2 D(T_MEASURED = 25 IS = 8.00E-16)

.MODEL PNP1 PNP (TREF = 25 IS = 8.00E-16 BF = 16362.72727)
.MODEL PNP2 PNP (TREF = 25 IS = {ISM2} BF = {BFM2})

.PARAM
+ C1    = 2.14E-10
+ C2    = 8.41E-10
+ CE    = 0.00E+00
+ GCM   = 5.51E-07
+ GA    = 1.74E-02
+ GB    = 2.29
+ GC    = 1.18E+04
+ ITL   = 9.00E-04
+ RC1   = 57.34
+ RC    = 8.48E-05
+ RE1   = 0.24
+ RE    = 2.22E+05
+ RO1   = 50
+ RO2   = 25
+ RP    = 4.40E+04
+ VC    = 1.80363
+ VE    = 1.80364
+ VTL   = 1.00E+00
+ VRC   = 1.35
+ ICE   = 509.1E-6
+ ISM2 = 8.149105E-16
+ BFM2 = 19998.88889

.ends njm4558_s
*$
```

BIPOLAR MODEL

| Pspice model parameter	Model description
T_MEASURED	Measured temperature
IS	saturation current
BF	ideal maximum forward beta
U0	Surface Mobility

Output Voltage Swing (VOM　High Side)

Output Voltage(VOMHigh Side)
### $V^+=15.0V, V^-=-15.0V, RL=10k$
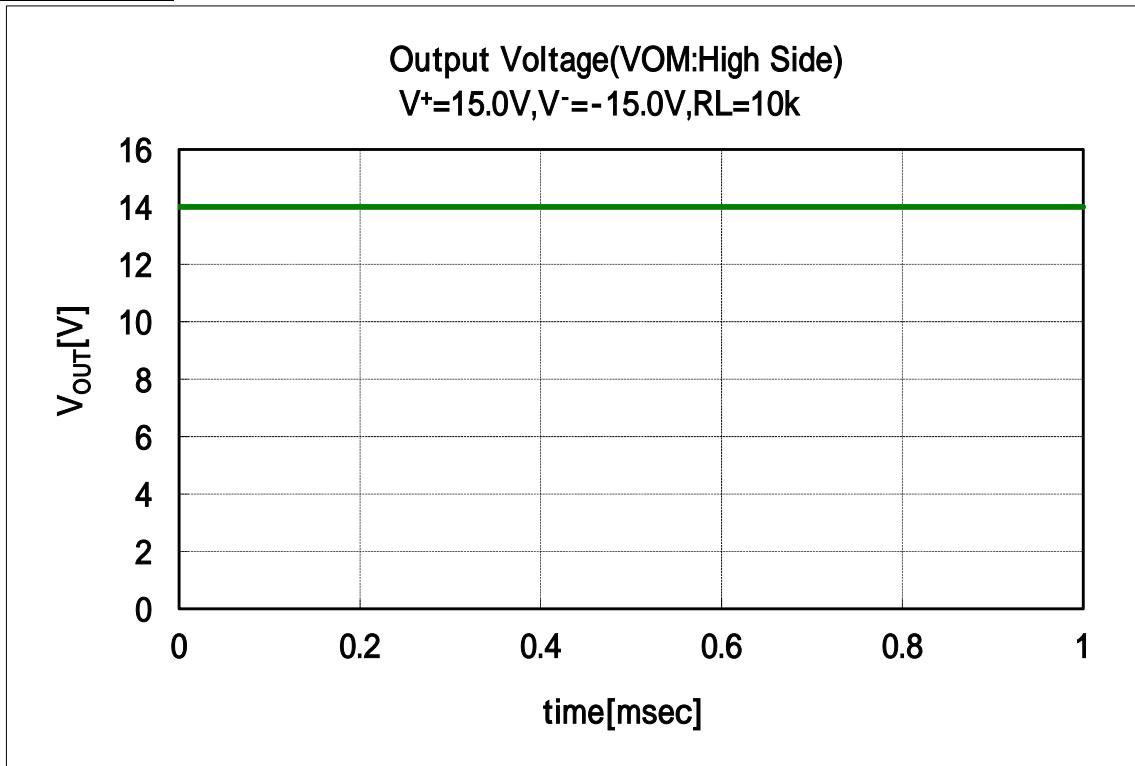
Evaluation circuit
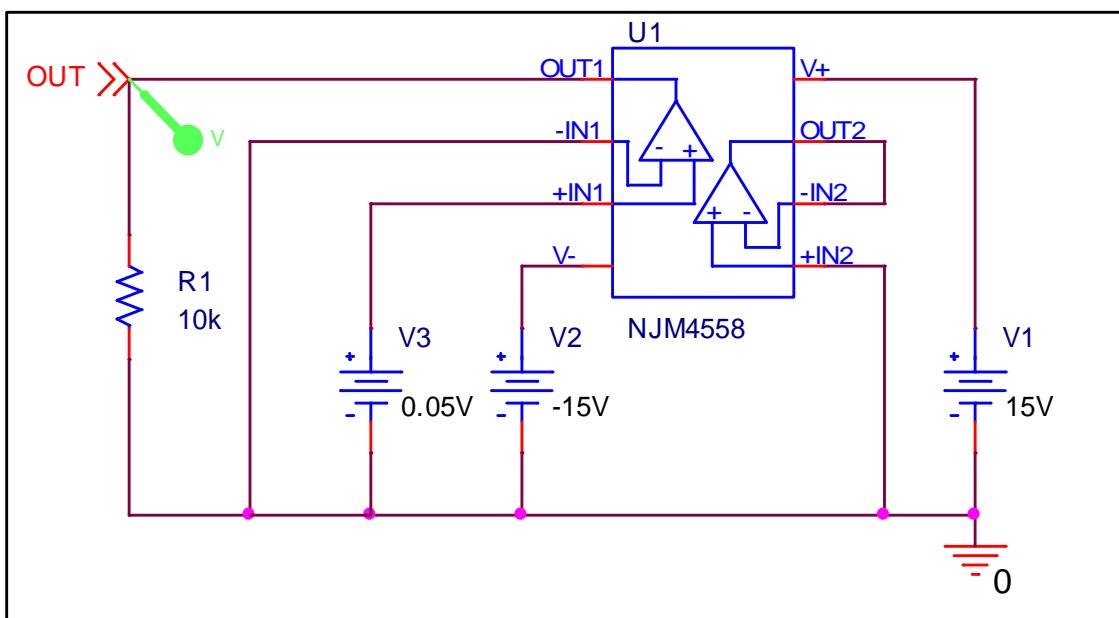
VOM(V)	Data sheet	Simulation	%Error
	14.0	14.0	0.0

Output Voltage Swing (VOM　Low Side)

Simulation result

Output Voltage(VOM Low Side)
V⁺=15.0V,V⁻=-15.0V,RL=10k
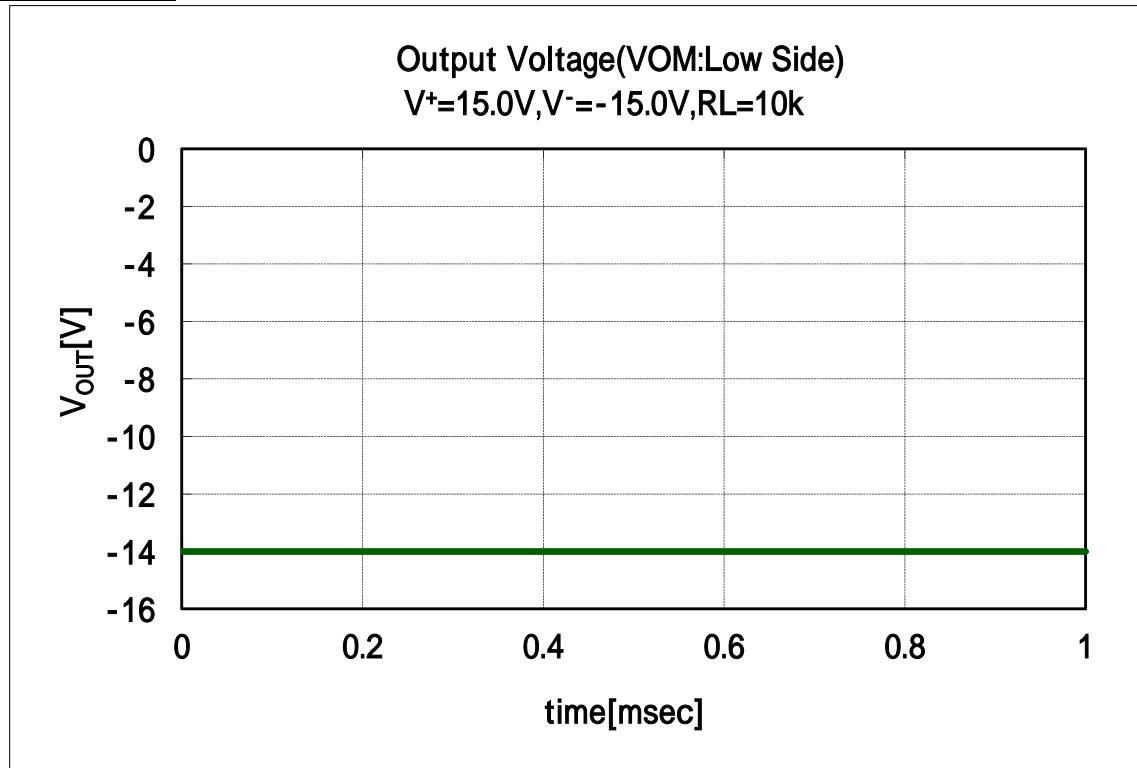
Evaluation circuit
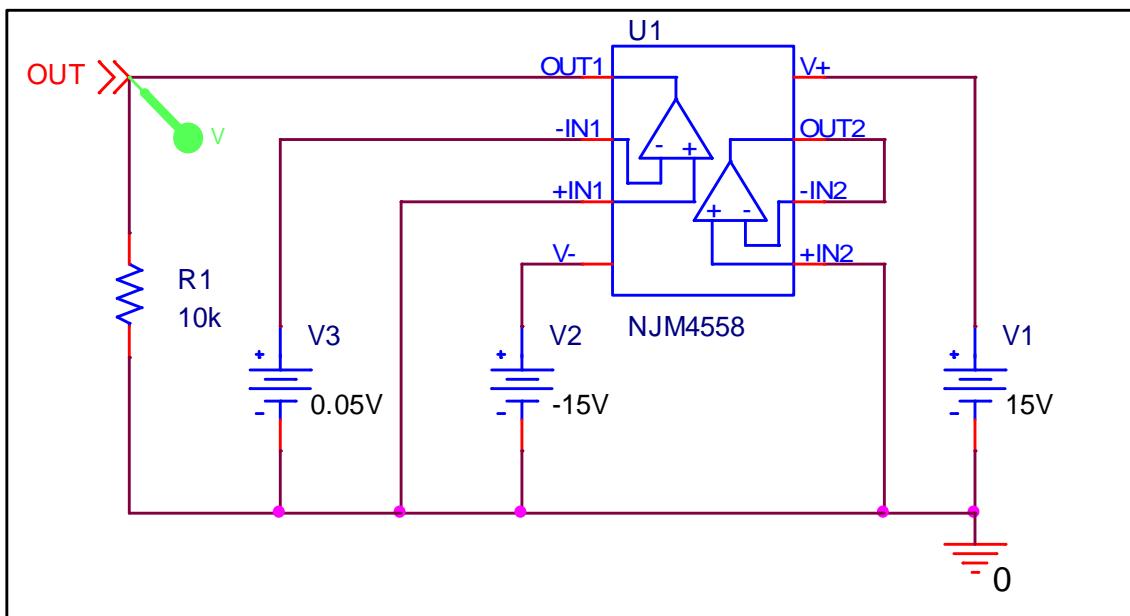
VOM(V)	Data sheet	Simulation	%Error
	-14.0	-14.0	0.0

Input Offset Voltage (VIO)

Offset Voltage(VIO)
$V^+=15.0V, V^-=-15.0V, RL=10k$
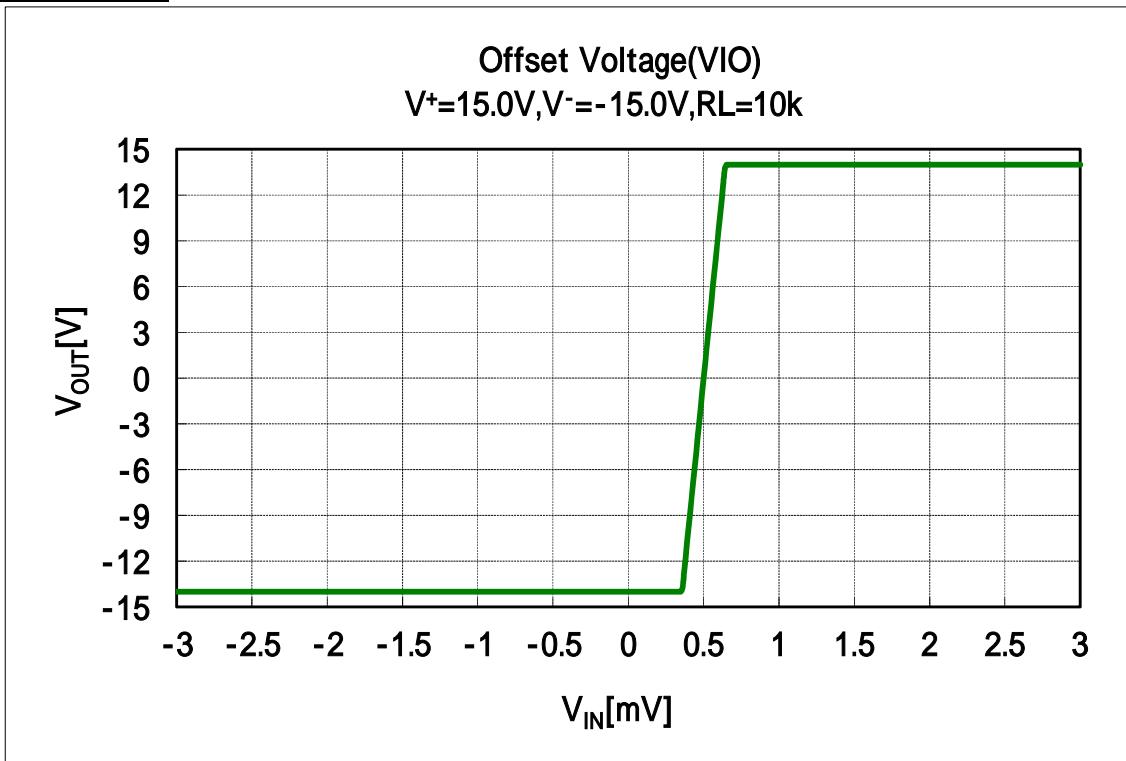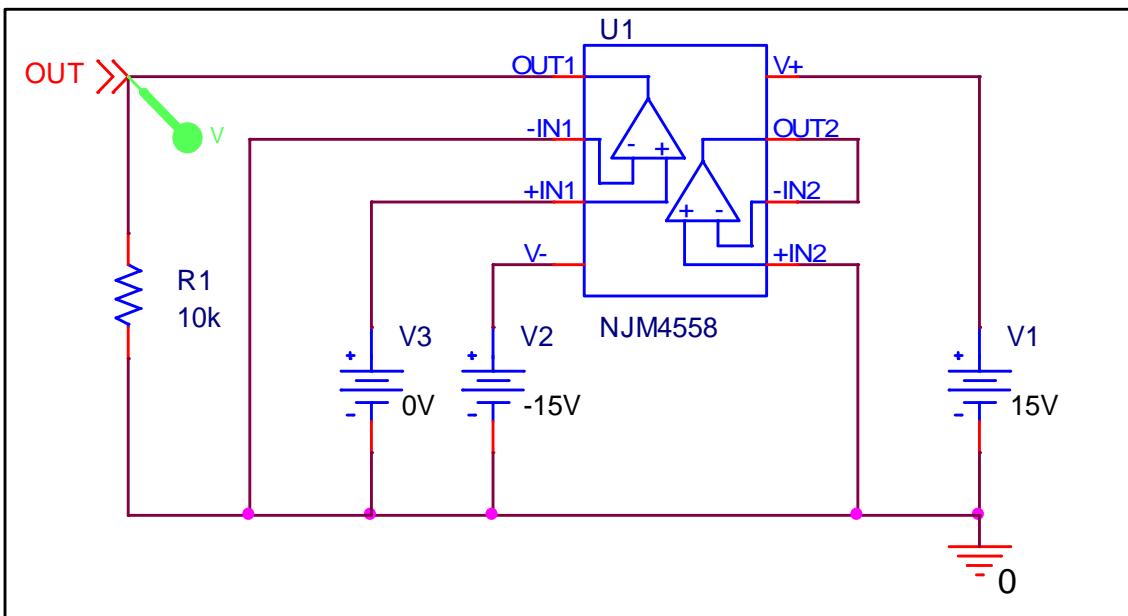
VIO(mV)	Measurement	Simulation	%Error
	0.5	0.5	0.0

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NJM4558

Slew Rate (+SR, -SR)

Simulation result

SlewRate(SR)
$V^+=15.0V, V^-=-15.0V, V_{IN}=1.0Vpp, RL=Open$

Evaluation circuit

NJM4558

V4
V1 = -0.5V
V2 = 0.5V
TD = 1u
TR = 1n
TF = 1n
PW = 2u
PER = 5u

V2 -15V

V1 15V

V3 0V

PARAMETERS:
V_OFF = 500.00812uV
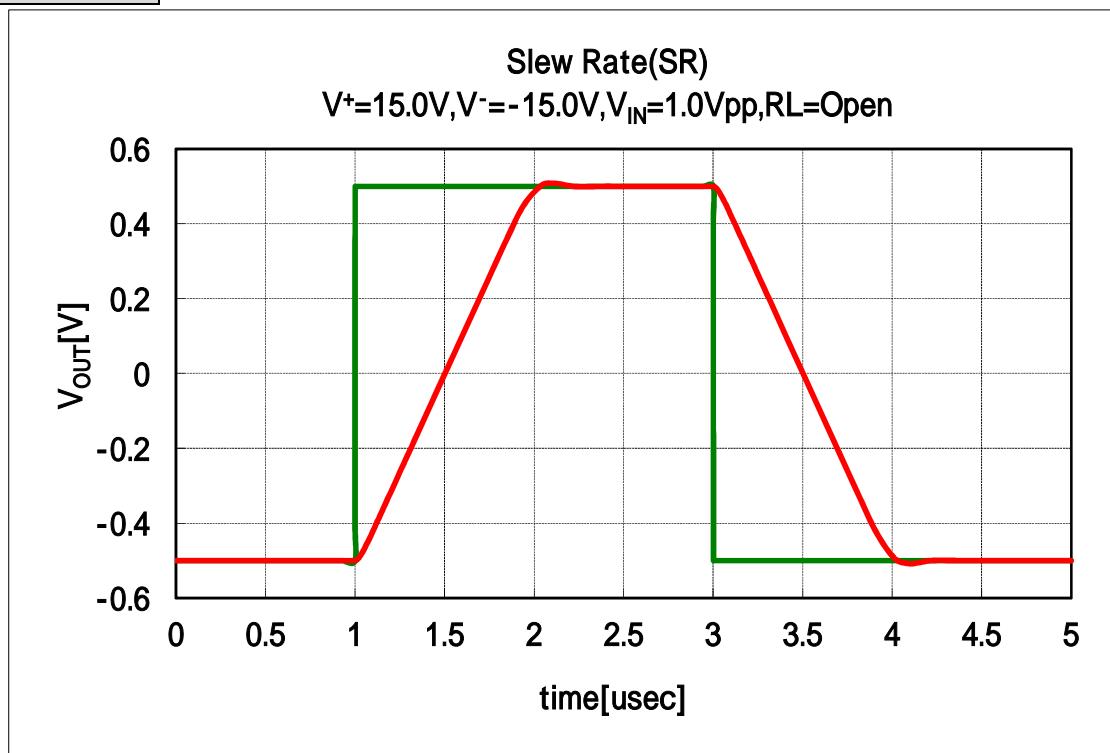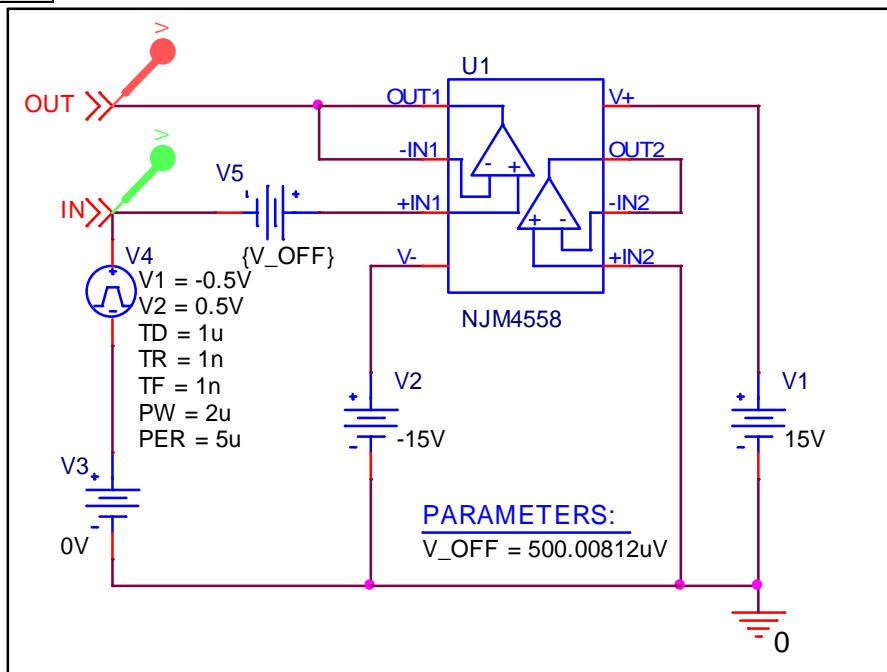
Slew Rate	Data sheet	Simulation	%Error
+SR(V/usec)	1.0	1.045	4.500
-SR(V/usec)	-1.0	-1.048	4.800

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Date:2016-6-10

## Open Loop Voltage Gain (AV)

Simulation result

Openloop Gain(AV)
$V^+=15.0V, V^-=-15.0V, RL=2k$
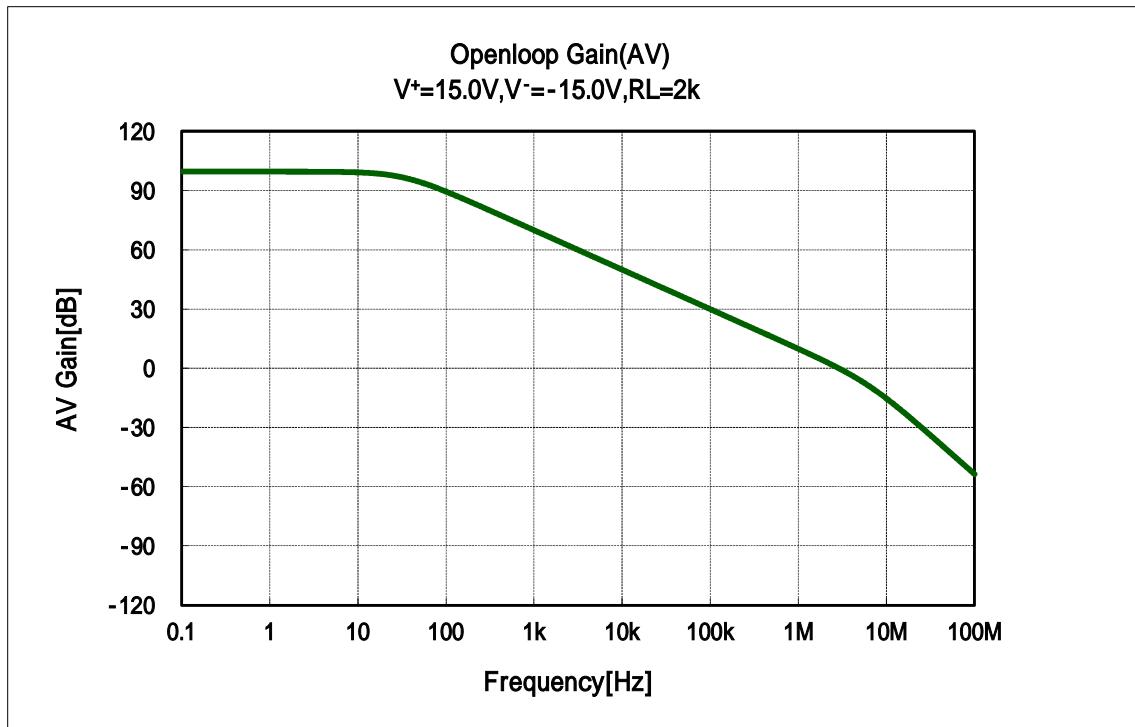
Evaluation circuit
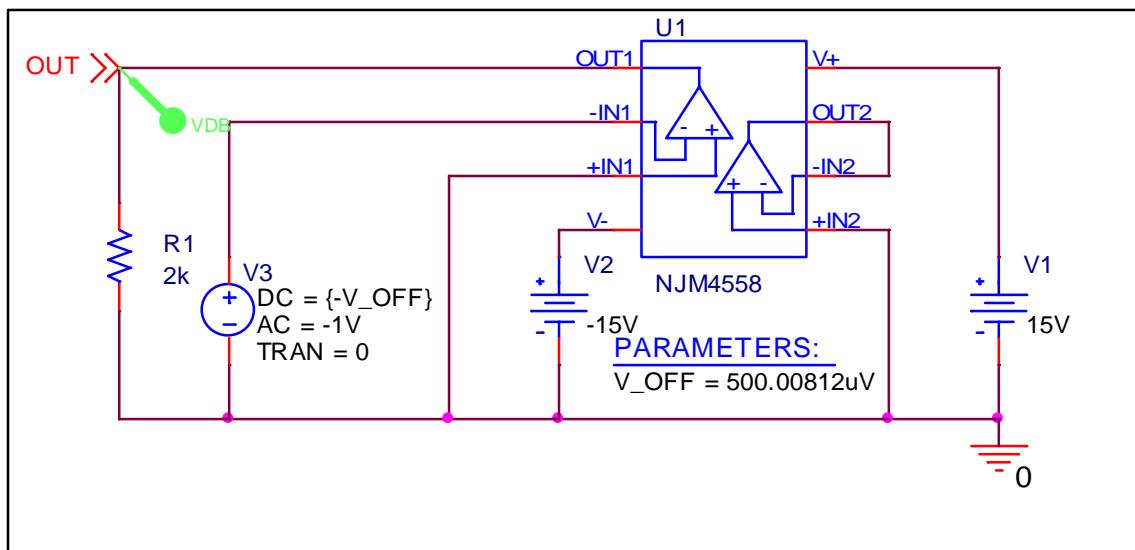
	Data sheet	Simulation	%Error
Av (dB)	100	99.559	0.441

Date:2016-6-10

Open Loop Voltage Gain (GBW , PM)

Simulation result

Openloop Gain(GBW,PM)
V⁺=15.0V,V⁻=-15.0V,RL=Open
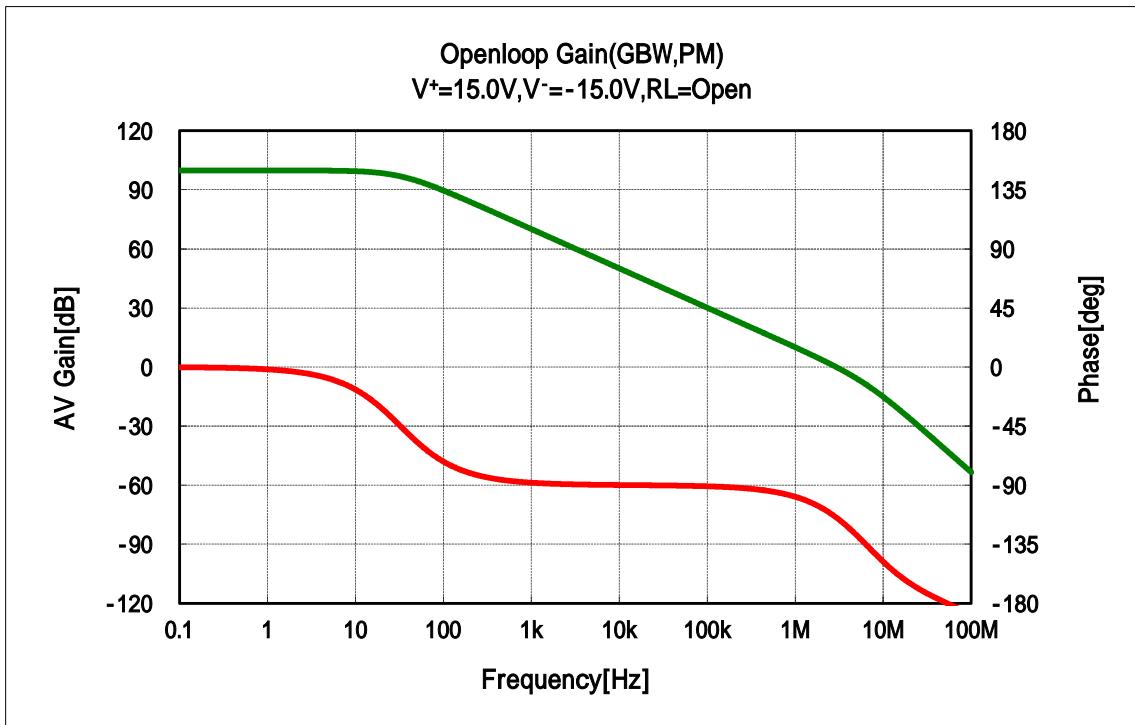
Evaluation circuit
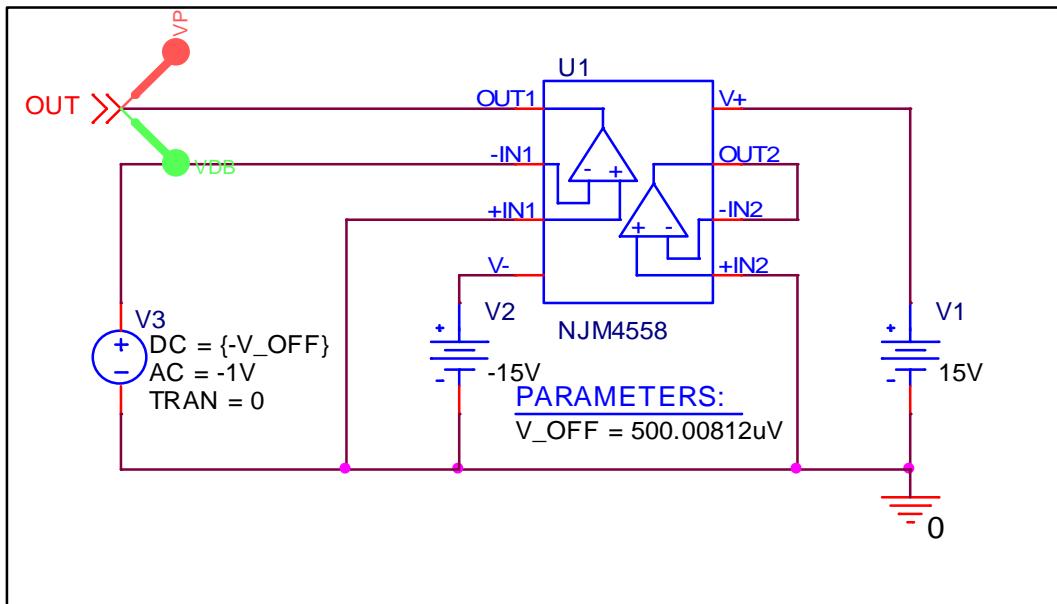
	Data sheet	Simulation	%Error
GBW(MHz)	3.0	2.921	2.633
PM(deg) * Reference value	-	65.365	-

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Date:2016-6-10

Common-Mode Rejection Ratio (CMR)

Simulation result

Common- Mode Rejection Ratio(CMR)
$V^+=15.0V, V^-=-15.0V, RL=10k$

Evaluation circuit

$$A_{CM} = \frac{V_{pp}(V_{out})}{V_{pp}(V_{inm})} = 3.135 = 9.925 [dB],$$
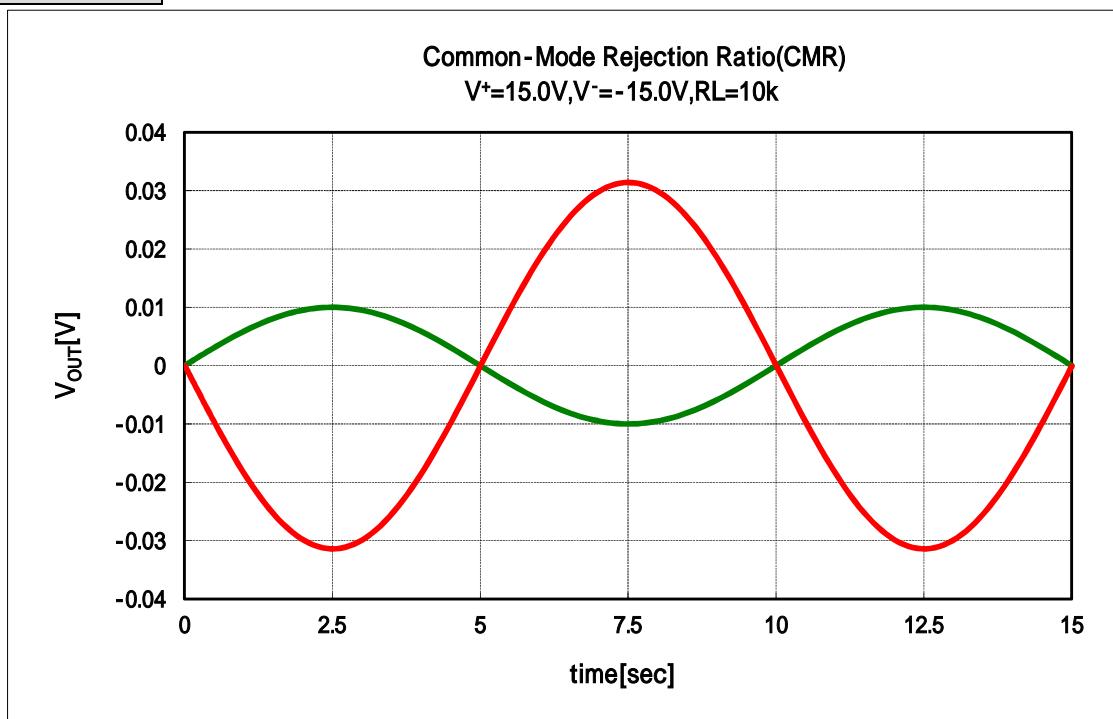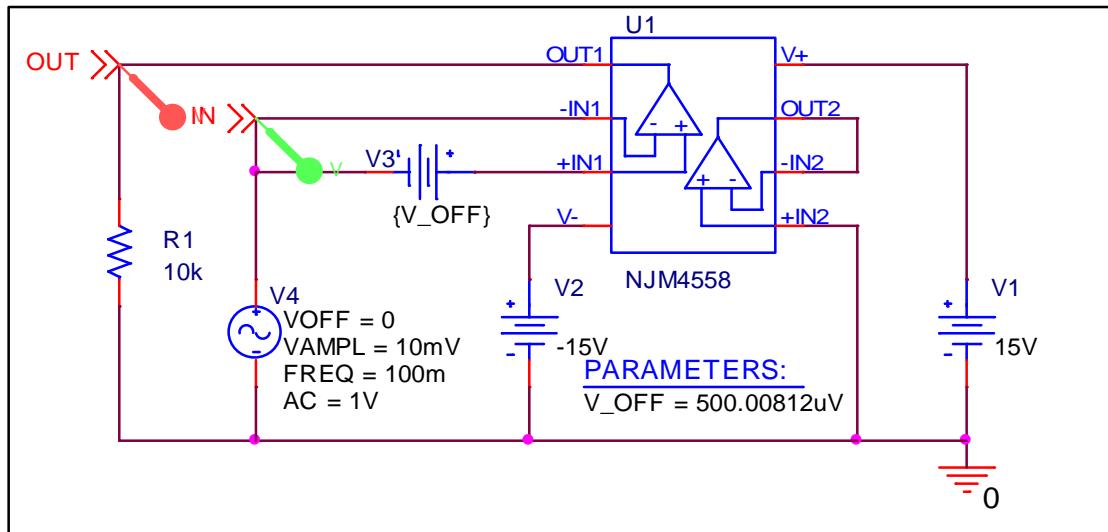
$$CMR = \left|\frac{A_{VD}}{A_{CM}}\right| = 99.559 - 9.925 = 89.634 [dB]$$

CMR(dB)	Data sheet	Simulation	%Error
	90	89.634	0.407

Input Bias Current (IB)

Simulation result

Input Bias Current(IB)
$V^+=15.0V, V^-=-15.0V, RL=10k$

(graph: Input Bias Current[nA] vs time[msec])

Evaluation circuit

(circuit diagram: U1 NJM4558, OUT, R1 10k, V2 -15V, V1 15V)
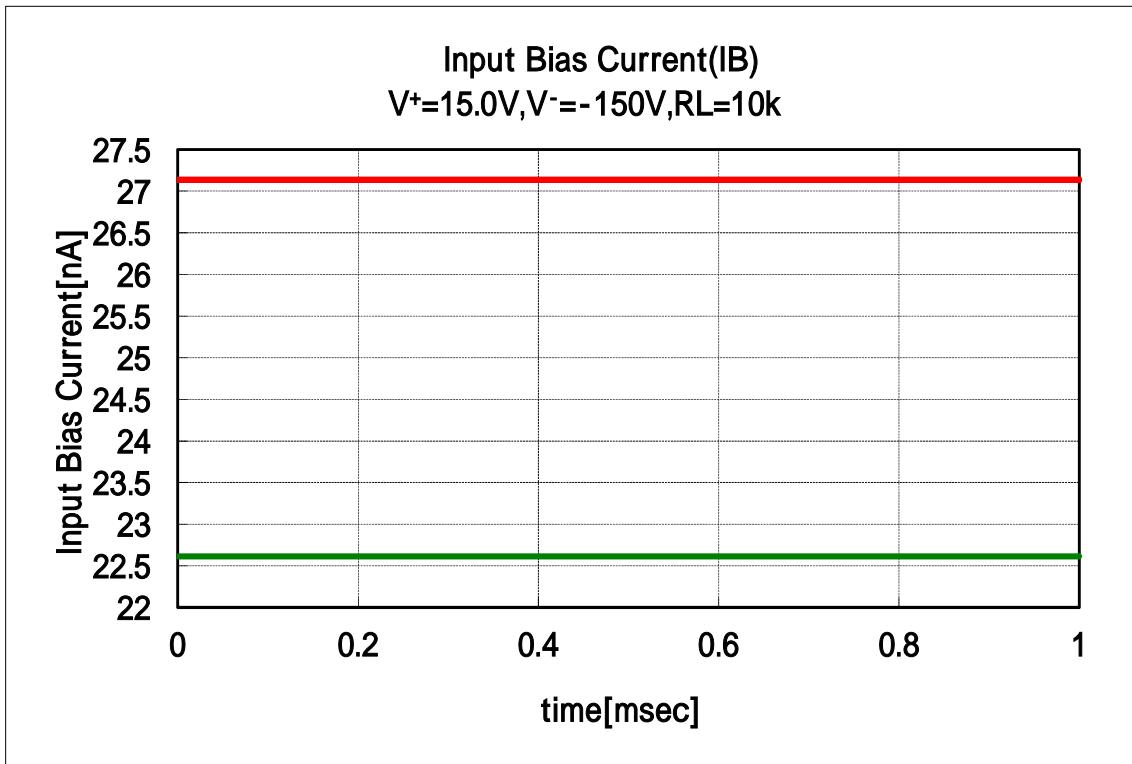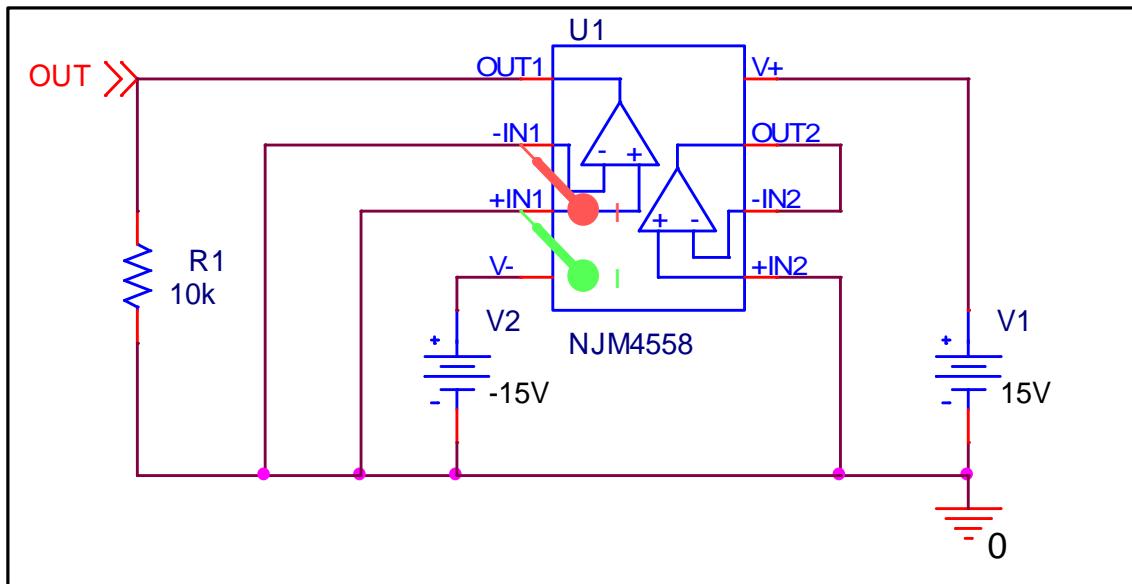
Input Bias Current	Data sheet	Simulation	%Error
IB+(nA)	25	22.614	9.544
IB-(nA)	25	27.138	8.552

Date:2016-6-10

Input Offset Current (IIO)

Simulation result

Input Offset Current(IIO)
$V^+=15.0V, V^-=-15.0V, RL=10k$
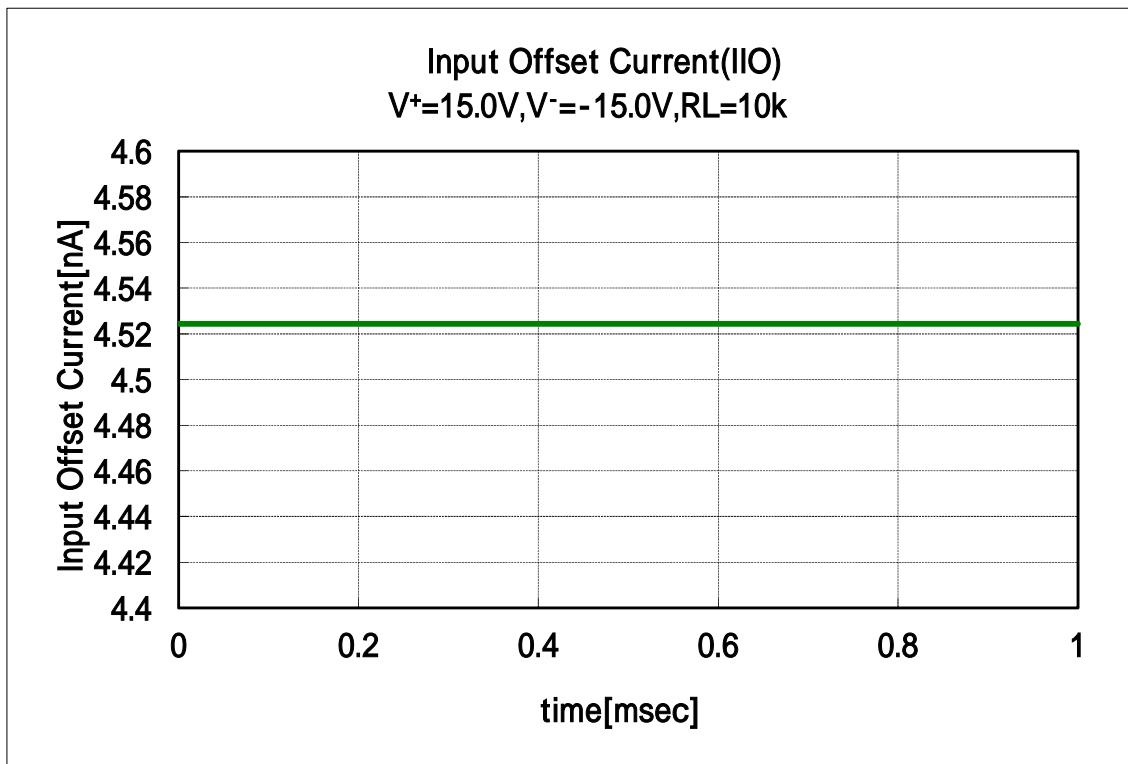
Evaluation circuit
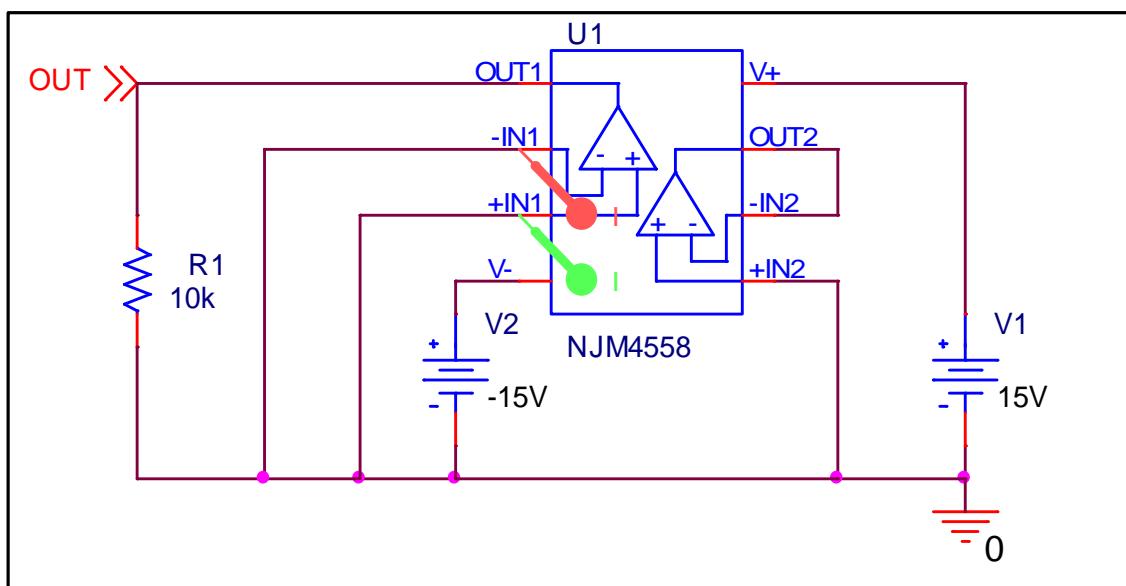
IIO(nA)	Data sheet	Simulation	%Error
	5	4.524	9.520